REMARKS

Reconsideration of this application, as amended, is respectfully requested.

Claims 1-6, and 8-14 are pending. Claims 1-6, and 8-14 stand rejected.

Claims 1 and 13 have been amended. No claims have been cancelled. Claim 15 has been added. Support for the amendments is found in the specification, the drawings, and in the claims as originally filed. Applicants submit that the amendments do not add new matter.

Rejections Under 35 U.S.C. § 103(a)

Claims 1, and 8-11 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,814,861 of Schunke et al. ("Schunke"). Claim 2 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Schunke in further view of U.S. Patent No. 5,970,351 of Takeuchi ("Takeuchi"). Claim 3 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Schunke in further view of U.S. Patent No. 6,057,582 of Choi ("Choi '582"). Claim 4 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Schunke in view of Takeuchi in further view of Choi '582. Claims 5 and 6 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Schunke in further view of U.S. Patent No. 5,793,088 of Choi et al. (Choi '088). Claim 12 stands rejected under 35 U.S.C. 103 § 103(a) as being unpatentable over Schunke in further view of U.S. Patent No. 5,567,966 of Hwang ("Hwang"). Claim 13 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Schunke in view of U.S. Patent No. 6,274,894 of Wieczorek et al. ("Wieczorek") in further view of Takeuchi. Claim 14 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Schunke in view of Wieczorek in view of Takeuchi and in further view of Choi '582.

As for claims 1, and 8-11 the Examiner has stated that

> Schunke discloses (see, for example, FIG 4) a transistor (device) comprising a gate dielectric, substrate (first conductivity region of a substrate), gate electrode, pair of sidewall spacers, and source and drain regions (a pair of silicon or silicon alloy inwardly concaved source/drain of a second conductivity type formed in said substrate). The source and drain regions are inwardly concaved and bend (inflection points) directly underneath the gate electrode. The channel region 5 directly beneath the gate electrode is larger that the channel region between the inflection points.

(p. 2, Office Action 120104)

Applicants respectfully disagree. Applicants have amended claim 1 to particularly point out that a pair of silicon or silicon alloy inwardly concaved regions formed in a substrate have metallurgical inflection points directly beneath the lower portion of the gate electrode extending the greatest distance laterally beneath the lower portion of the gate electrode at the inflection points between 50-250Å laterally beneath the gate electrode and at a depth of between 25-100Å beneath the gate dielectric, the metallurgical inflection points define a metallurgical channel length directly beneath the lower portion of the gate electrode, wherein the metallurgical channel length directly beneath the gate dielectric is larger than the metallurgical channel length between the inflection points.

Amended claim 1 reads as follows:

A device comprising:
a gate dielectric formed on first conductivity region of a substrate;
a gate electrode formed on said gate dielectric, said gate electrode having a lower portion formed directly on said gate dielectric;
a pair of sidewall spacers formed along laterally opposite sidewalls of said gate electrode; and
a pair of silicon or silicon alloy inwardly concaved source/drain regions of a second conductivity type formed in said substrate and on opposite sides of said gate electrode creating metallurgical inflection points directly beneath said lower portion of said gate electrode formed directly on said gate dielectric layer, wherein said silicon or silicon alloy source/drain regions extend the greatest distance laterally beneath said lower portion of the gate electrode at said inflection points which occurs between 50-250Å laterally beneath said gate electrode and at a depth of between 25-100Å beneath said gate dielectric and define a metallurgical channel length directly beneath said lower portion of said gate electrode in said first conductivity type region, and wherein said metallurgical channel length directly beneath said lower portion of said gate electrode is larger than said metallurgical channel length between said inflection points.

(Amended claim 1) (emphasis added)

Schunke discloses a U.S. patent 5, 041,885 to Gualandris et al. ("Gualandris"), discussed as a reference in previous office actions. Schunke discloses a distribution profile of dopants, which has a curvature, in a substrate. More specifically, Shunke discloses

> More specifically, referring to FIG. 2, U.S. Pat. 5,041,885 to Gualandris et al. uses implantation and diffusion to create the source/drain regions along the vertical edges of the transistor gate. A dopant species is first implanted in the substrate and then diffused as shown in FIG. 2. This creates a doping profile with a Gaussian distribution, as diffusion of dopant is equal in all directions. That is, there is essentially a 1:1 ratio of movement along both the X and Y axes. As a result, the respective boundary between each of the source/drain regions and the channel region has a curvature of substantially constant radius throughout the extent of the semiconductor substrate between the source/drain regions and the gate electrode.

(Schunke, col. 2, lines 44-55) (emphasis added).

In particular, Schunke discloses

> In the GDD technique, the dopant species are first implanted in regions of the substrate defined by the oxide spacers, as shown in FIG. 3 (a), and then diffused, as shown in FIG. 3 (b). A second implantation and diffusion is then carried out creating contours of equal ion concentration having a Gaussian distribution, as shown in FIG. 4.

(Schunke, col.3, lines 24-29) (emphasis added)

Thus, Schunke, in contrast, discloses contours of equal dopant concentration in a silicon substrate and does not disclose, teach, or suggest metallurgical inflection points created by a pair of silicon or silicon alloy inwardly concaved regions formed in a substrate directly beneath the lower portion of the gate electrode extending the greatest distance laterally beneath the lower portion of the gate electrode at the inflection points between 50-250Å laterally beneath the gate electrode and at a depth of between 25-100Å beneath the gate dielectric, which define a metallurgical channel length directly beneath the lower portion of the gate electrode, wherein the metallurgical channel length directly beneath the gate dielectric is larger than the metallurgical channel length between the inflection points, as recited in amended claim 1.

It is respectfully submitted that Schunke does not disclose, teach, or suggest optimization of a transistor to have metallurgical inflection points created by inwardly concaved silicon or silicon alloy regions formed in the substrate, which define a metallurgical channel length directly beneath the lower portion of the gate electrode, wherein the metallurgical channel length directly

beneath the gate dielectric is larger than the metallurgical channel length between the inflection points, as recited in amended claim 1.

Furthermore, even if Schunke were optimized as the Examiner suggested, to have an inflection point between 50-250Å laterally beneath the gate electrode and at a depth of between 25-100Å beneath the gate dielectric, such an optimization would still lack of metallurgical inflection points that define a metallurgical channel length directly beneath the lower portion of the gate electrode, wherein the metallurgical channel length directly beneath the gate dielectric is larger than the metallurgical channel length between the inflection points, as recited in amended claim 1.

Therefore, applicants respectfully submit that claim 1 is not obvious under 35 U.S.C. §103(a) over Schunke.

Given that claims 2-6 and 8-12 depend, directly or indirectly, on claim 1 and add additional limitations, applicants respectfully submit that claims 2-12 are likewise not obvious under 35 U.S.C. §103(a) over Schunke.

Similarly to Schunke, neither Takeuchi, Choi'582, Choi'088, Hwang, nor Wieczorek discloses, teaches, or suggests the limitation of amended claim 1 of metallurgical inflection points created by a pair of silicon or silicon alloy inwardly concaved regions formed in a substrate directly beneath the lower portion of the gate electrode extending the greatest distance laterally beneath the lower portion of the gate electrode at the inflection points between 50-250Å laterally beneath the gate electrode and at a depth of between 25-100Å beneath the gate dielectric, which define a metallurgical channel length directly beneath the lower portion of the gate electrode, wherein the metallurgical channel length directly beneath the gate dielectric is larger than the metallurgical channel length between the inflection points.

Takeuchi, in contrast, discloses elevated drain/source regions without inflection points, only beneath the vertical sidewall isolators of the gate electrode, aiming at the ideal junction depth of zero.

Choi_1, in contrast, discloses conventional drain/source regions without inflection points, formed merely at both sides, and not underneath the gate electrode.

Choi_2, in contrast, discloses source/drain regions without inflection points, formed merely at both sides of a gate electrode and underneath isolating sidewalls, and not underneath the gate electrode.

Hwang, in contrast, discloses elevated source/drain regions without inflection points, having conventional LDD portions at both sides of a gate electrode.

Wieczorek, in contrast, discloses source and drain regions without inflection points, with low-bandgap portions that merely underlie sidewall spacers of the gate electrode (see, for example, Fig. 10).

Hence, none of the references cited by the Examiner discloses, teaches, or suggests the limitations of claim 1 metallurgical inflection points created by a pair of silicon or silicon alloy inwardly concaved regions formed in a substrate directly beneath the lower portion of the gate electrode extending the greatest distance laterally beneath the lower portion of the gate electrode at the inflection points between 50-250Å laterally beneath the gate electrode and at a depth of between 25-100Å beneath the gate dielectric, which define a metallurgical channel length directly beneath the lower portion of the gate electrode, wherein the metallurgical channel length directly beneath the gate dielectric is larger than the metallurgical channel length between the inflection points.

Consequently, even if Schunke, Takeuchi, Choi'582, Choi'088, Hwang, and Wieczorek were combined, such a combination would lack such limitation of amended claim 1.

Therefore, applicants respectfully submit that amended claim 1 is not obvious under 35 U.S.C. § 103 (a) over the above references.

Given that claims 2-6 and 8-12 depend from amended claim 1, either directly or indirectly, and add additional limitations, applicants respectfully submit that claims 2-6 and 8-12 are not obvious under 35 U.S.C. §103 (a) over Schunke, in view of Takeuchi, in view of Choi'582, in view of Choi'088, in view of Hwang, and further in view of Wieczorek.

Because amended independent claim 13 and new claim 15 contain at least the same limitations as amended claim 1, applicants respectfully submit that claims 13 and 15 are likewise not obvious under 35 U.S.C. §103(a) over the references cited by the Examiner.

Given that claim 14 depends directly from claim 13 and add additional limitations, applicants respectfully submit that claim 14 is likewise not obvious under 35 U.S.C. §103(a) over the references cited by the Examiner.

It is respectfully submitted that in view of the amendments and arguments set forth herein, the applicable rejections and objections have been overcome. If there are any additional charges, please charge Deposit Account No. 02-2666 for any fee deficiency that may be due.

Respectfully submitted,

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